IN THE CLAIMS:

Please cancel claims 6-13 and 17-25 without prejudice, resulting in the following listing of the claims. This listing replaces and supersedes all prior claim listings.

1. (Original) An operation-processing device for performing operation processing based on an arbitrary operation program, said device comprising:

a register array having plural registers each for holding an arbitrary value based on a write address and a write control signal and outputting this value based on a read address;

an operation portion for performing operation on a value read from said register array;

an instruction-decoding portion for decoding an operation instruction from an operation program for operating said operation portion; and

an instruction-execution-controlling portion for controlling said register array and the operation portion in order to execute an operation instruction decoded by said instruction-decoding portion,

wherein said instruction-execution-controlling portion selects one of said registers based on said operation instruction; and

wherein based on a value held by said selected register, said instruction-execution-controlling portion performs register-to-register addressing processing for selecting another register.

2. (Original) The operation-processing device according to claim 1, comprising a read only memory cell in which said operation program is stored.

3. (Original) The operation-processing device according to claim 1, wherein said operation program includes operation instruction to perform the register-to-register addressing processing.

4. (Original) The operation-processing device according to claim 1,

wherein said register array and the read only memory are comprised of plural memory cells;

wherein said operation portion, the instruction-decoding portion, and the instruction-execution-controlling portion are comprised of plural arithmetic/logic operation elements; and

wherein said memory cells and the arithmetic/logic operation elements are constituted of a programmable logic devices formed on the identical semiconductor chip.

5. (Original) The operation-processing device according to claim 1, wherein said instruction execution-controlling portion has:

a first selector for selecting any one of a read execution address to select said one register and a read address to select this register again; and

a second selector for selecting any one of a write execution address to select said one register and a write address to select this register again.

6-13 (Canceled).

14. (Original) An operation-processing method for performing operation processing based on an arbitrary operation program, said method comprising the steps of:

beforehand preparing plural registers each for holding an arbitrary value based on a write address and a write control signal and outputting this value based on a read address;

thereafter decoding an operation instruction from said operation program;

selecting one of said registers based on said operation instruction;

performing register-to-register addressing processing for selecting, based on a value held by said selected register, another register and selecting said another register based on said operation instruction; and

performing operation on a value held by said selected another register and a value of the register selected by said register-to-register addressing processing.

15. (Original) The operation-processing method according to claim 14, wherein a result of said operation is stored in the register selected on the basis of the value held by said register.

16. (Original) The operation-processing method according to claim 14, wherein said operation program includes operation instruction to perform said register-to-register addressing processing.

17-25 (Canceled).